

### Technical Data

S1310 / S1510 Series



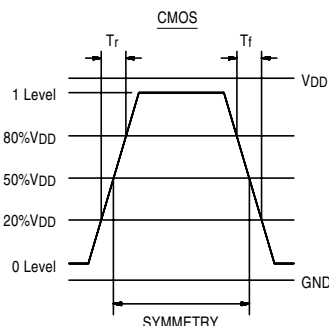
#### Description

A voltage controlled crystal oscillator with a wide range of performance options available up to 125 MHz. This economic part is designed for phase-locked loop circuits commonly encountered in telecom, LAN and wireless data, and in video processing applications. The HCMOS output can drive both high speed CMOS and TTL loads. The devices are packaged in either standard 14-pin or 8-pin DIP compatible all metal, resistance welded packages for commercial or industrial temperature range applications.

#### Applications & Features

- Wide frequency range up to 125 MHz
- HCMOS compatible
- ~ Full and half size standard DIP packages
- ~ Tri-state version available, see part numbering guide for options

#### Output Waveform



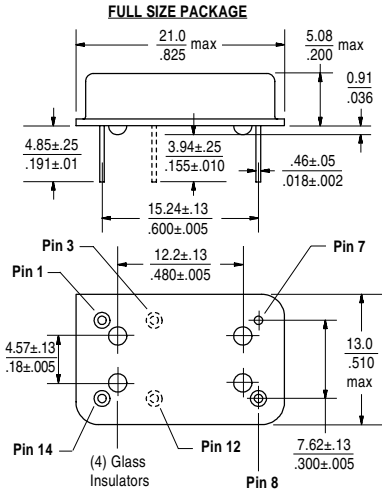
|                              |   |
|------------------------------|---|
| <b>Frequency Range:</b>      | 32 MHz to 125 MHz   |
| <b>Frequency Stability:</b>  | ±25 or ±50 ppm over all conditions: operating temperature, voltage change, load change, calibration tolerance, with VC = 2.5V @ 5V, VC = 1.65V @ 3.3V   |
| <b>Aging:</b>                | @ 40°C: ±10 ppm max for 5 years or ±12 ppm max for 10 years   |
| <b>Temperature Range:</b>    | Operating: 0 to +70°C, -40 to +85°C<br>Storage: -55 to +125°C   |
| <b>Supply Voltage:</b>       | Recommended Operating: 5V ±5% or 3.3V ±10%  |
| <b>Supply Current:</b>       | 32 to 70 MHz: 50mA max, 35mA max @ 3.3V<br>70+ to 125 MHz: 65mA max, 35mA max @ 3.3V  |
| <b>Output Drive:</b>         | Symmetry: 3.3V: 45/55% max @ 50% VDD for 0 to 70°C, 3.3V: 40/60% max @ 50% VDD for -40 to +85°C<br>5.0V: 45/55% max @ 50% VDD or 40/60% max @ 1.4V TTL level<br>Rise & Fall Times: 4ns max: 20% to 80% VDD<br>1.5ns max: 0.5V to 2.5V @ 5V TTL only<br>0.5V max @ 5V or 20% VDD max @ 3.3V<br>Logic 0: 2.5V min @ 5V or 80% VDD min @ 3.3V<br>Logic 1: 5V: 5TTL or 50pF, 32 to 50 MHz<br>5V: 5TTL or 30pF 50+ to 125 MHz<br>3.3V: 30pF up to 80 MHz, 95Ω AC up to 125 MHz<br>Jitter: 20ps max RMS period jitter |
| <b>Pull Characteristics:</b> | Input Impedance: 50KΩ min<br>Frequency Response (-3dB): 50 kHz min<br>Pullability: ±25, ±50, ±75, ±100 ppm APR*<br>Control Voltage: 0.5 to 4.5V @ 5V or 0.3 to 3.0V @ 3.3V<br>Transfer Function: Frequency increases when Control Voltage increases<br>Linearity: 5% or 10% max<br>Center Control Voltage: 2.5V @ 5V, 1.65V @ 3.3V  |
| <b>Mechanical:</b>           | Shock: MIL-STD-883, Method 2002, Condition B<br>Solderability: MIL-STD-883, Method 2003<br>Terminal Strength: MIL-STD-202, Method 211, Conditions A and C<br>Vibration: MIL-STD-883, Method 2007, Condition A<br>Solvent Resistance: MIL-STD-202, Method 215<br>Resistance to Soldering Heat: MIL-STD-202, Method 210, Condition A, B or C  |
| <b>Environmental:</b>        | Gross Leak Test: MIL-STD-883, Method 1014, Condition C<br>Fine Leak Test: MIL-STD-883, Method 1014, Condition A2<br>Thermal Shock: MIL-STD-883, Method 1011, Condition A<br>Moisture Resistance: MIL-STD-883, Method 1004   |

\* APR = (VCXO Pull relative to specified Output Frequency) – (VCXO Frequency Stability)

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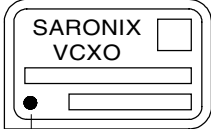
#### Package Details



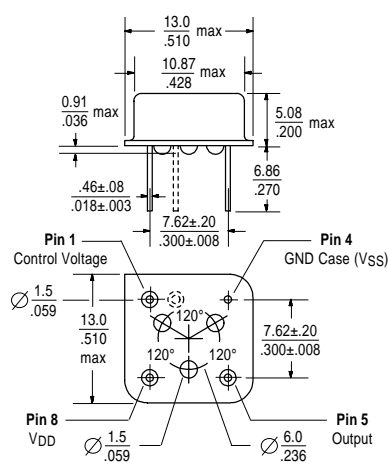
**Pin Function:**  
 Pin 1: Control Voltage  
 Pin 3: Tri-State control (Tri-State version only)  
 Pin 7: GND / Case (VSS)  
 Pin 8: Output  
 Pin 12: N/C (Tri-State version only)  
 Pin 14: VDC (VDD)

#### Standard Marking Format

Includes Date Code, Frequency & Model



#### HALF SIZE PACKAGE



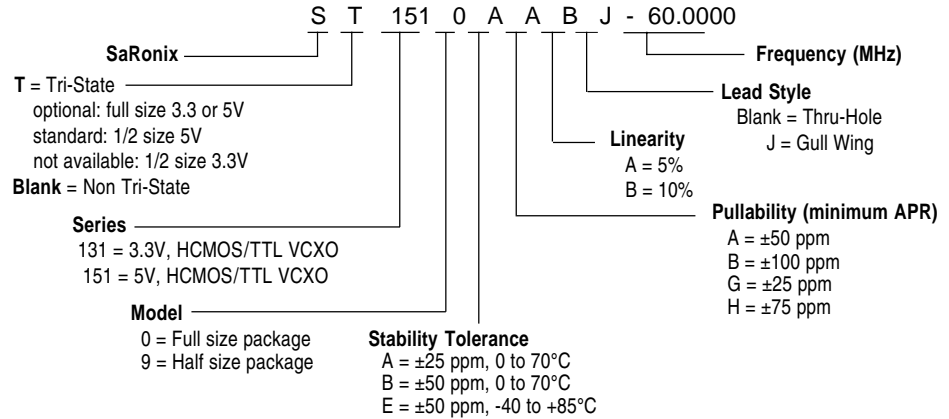
#### Standard Marking Format

Includes Date Code, Frequency & Model



Scale: None (Dimensions in mm / inches)

#### Part Numbering Guide



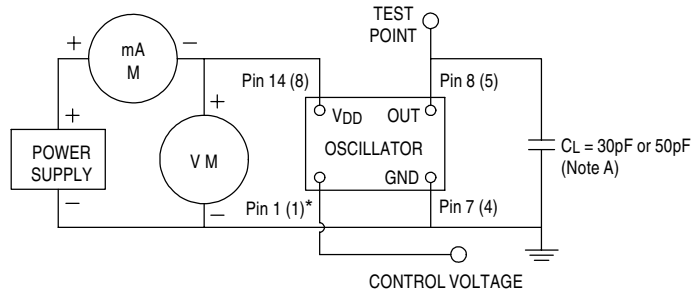
#### Tri-State Logic Table

| Pin 3 Input    | Pin 8 Output   |
|----------------|----------------|
| Logic 1 or NC  | Oscillation    |
| Logic 0 or GND | High Impedance |

Required Input Levels on Pin 3:

Logic 1 = 3.0V min  
 Logic 0 = 0.3V max

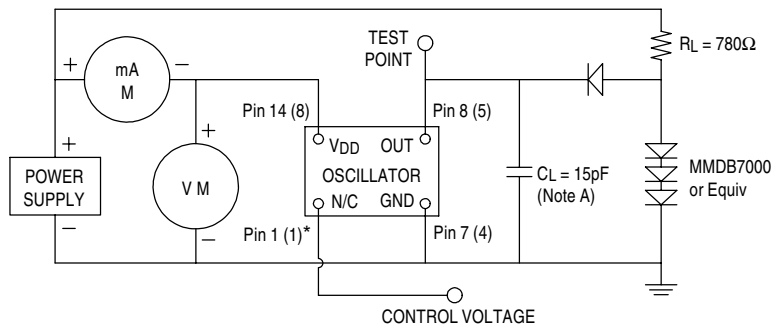
#### Test Circuits



NOTE A: CL includes probe and fixture capacitance (50pF max 32 to 50 MHz, 30pF max 50+ to 125 MHz)

\* ( ) Indicates pin numbers for half size package

Figure 1 – 30pF or 50pF load Test Circuit



NOTE A: CL includes probe and fixture capacitance

\* ( ) Indicates pin numbers for half size package

Figure 2 – TTL load Test Circuit

All specifications are subject to change without notice.

DS-162 REV D

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