

Technical Data

S1318/1518 Series



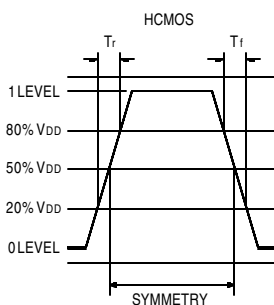
Description

A voltage controlled crystal oscillator, with output logic levels compatible with HCMOS and TTL logic families. The device is packaged in a 6-pin, SMD, J leaded package. The plastic molded surface mountable package is ideal for today's automated assembly environments. This product family is compatible with AT&T "S" series VCXOs.

Applications

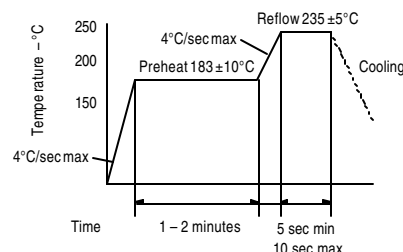
- For use in phase-locked loop (PLL) clock and data recovery, frequency translation, or frequency synthesis applications in video, video compression, telephony, and LAN/WAN data communication environments.
- High and wide frequency range from 32 MHz to 120 MHz
- 3 and 5 Volt operation
- Compact, plastic molded surface mount package
- HCMOS and TTL compatible
- Tri-state output

Output Waveform



Frequency Range:	32 MHz to 120 MHz
Frequency Stability:	±50 ppm over all conditions: operating temperature, voltage change, load change, calibration tolerance, aging, with $V_C = 2.5V @ 5V$, $V_C = 1.65V @ 3.3V$
Temperature Range:	Operating: 0 to +70°C (-40 to +85°C available) Storage: -55 to +125°C
Supply Voltage:	Recommended Operating: +5 VDC ±5% or 3.3V ±10%
Supply Current:	32 to 70 MHz: 50mA max, 35mA max @ 3.3V 70+ to 120 MHz: 65mA max, 35mA max @ 3.3V
Output Drive:	Symmetry: 45/55% @ 50% VDD (3V: 0 to +70°C) 40/60% @ 1.4V level (3V @ 50% VDD -40 to +85°C) Rise & Fall Times: 4ns max, 20 to 80% VDD 1.5ns max, 0.5V to 2.5V (@ 5V and TTL load only) Logic 0: 0.5V max, 20% VDD max @ 3.3V Logic 1: 2.5V min, 80% VDD max @ 3.3V Load: 50pF or 5TTL: 32 to 50 MHz, 3.3V: 30pF up to 80 MHz 30pF or 5TTL: 50+ to 120 MHz, 3.3V: 95ΩAC up to 120 MHz Jitter: 25ps max RMS period jitter
Pull Characteristics:	Input Impedance: 50KΩ min Frequency Response (-3dB): 20 kHz min Pullability: ±25, ±50, ±75 ppm APR* (See Part Numbering Guide) Control Voltage: 0.5 to 4.5VDC, 0.3 to 3.0V Transfer Function: Frequency increases when Control Voltage increases Linearity: 10% max Center Control Voltage: 2.5V @ 5V, 1.65V @ 3.3V
Mechanical:	Shock: MIL-STD-883, Method 2002, Condition B Solderability: MIL-STD-883, Method 2003 Terminal Strength: MIL-STD-202, Method 211, Conditions A & C Vibration: MIL-STD-883, Method 2007, Condition A Solvent Resistance: MIL-STD-202, Method 215 Resistance to Soldering Heat: MIL-STD-202, Method 210, Condition I or J
Environmental:	Thermal Shock: MIL-STD-883, Method 1011, Condition A Moisture Resistance: MIL-STD-883, Method 1004

Solder Reflow Guide



* APR = (VCXO Pull relative to specified Output Freq. @ nominal control voltage) - (VCXO Freq. Stability)

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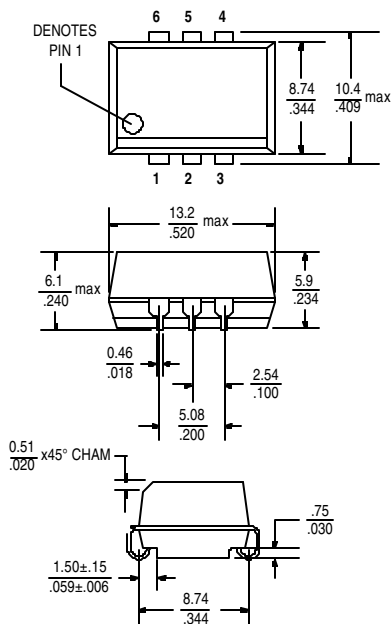
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Tri-State Logic Table

Pin 2 Input	Pin 4 Output
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance or Standby Function

Required Input Levels on Pin 2:
 Logic 1 = 3.0V min
 Logic 0 = 0.5V max

Package Details

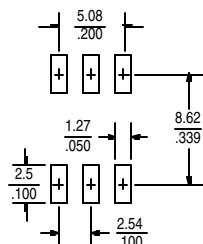


Pin Functions:

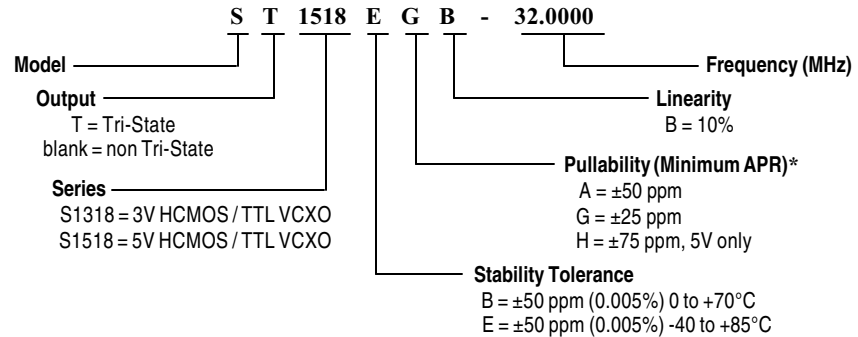
Pin 1: Control Voltage Pin 4: Output
 Pin 2: Tri-State Control Pin 5: N/C
 Pin 3: GND Pin 6: Vcc

Scale: None (Dimensions in $\frac{\text{mm}}{\text{inches}}$)

Recommended Land Pattern

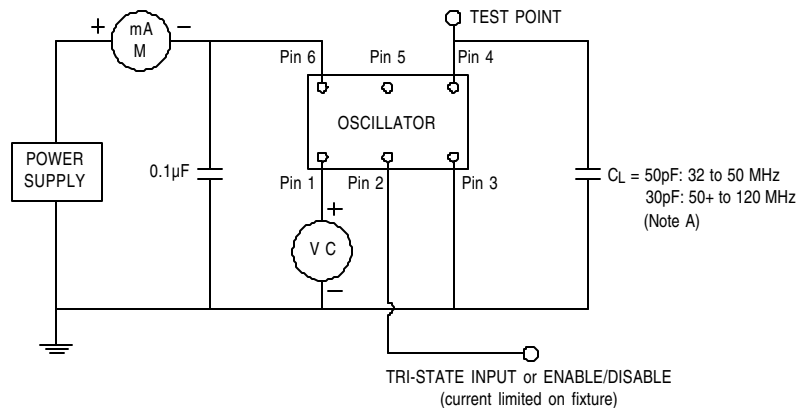


Part Numbering Guide

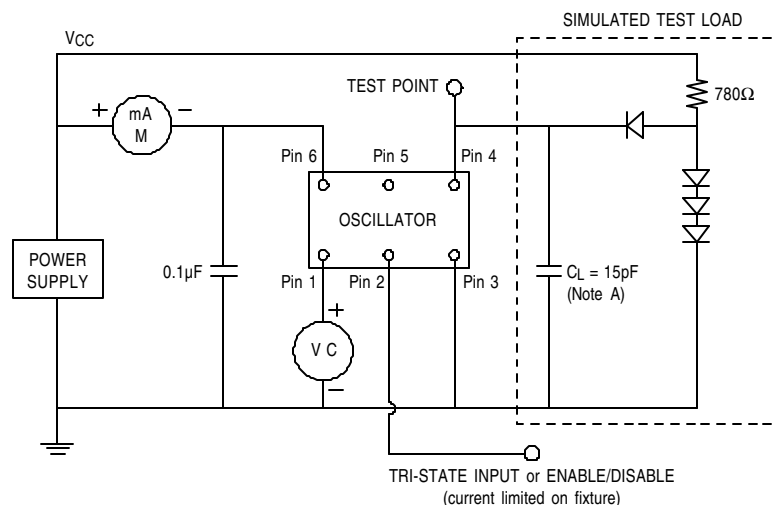


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Test Circuits:



NOTE A: CL includes probe and jig capacitance.



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All specifications are subject to change without notice.