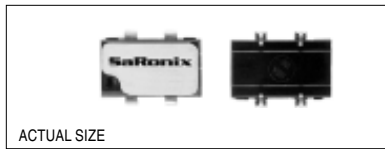


Technical Data

STA / STT Series, Type F



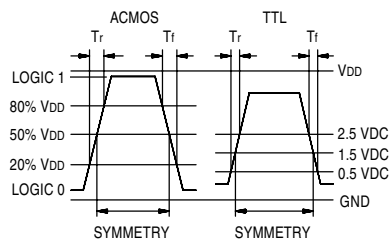
Description

A crystal controlled oscillator, available for 5V operation to drive HCMOS and NMOS microprocessors. This ACMOS device is capable of driving both HCMOS and TTL loads at high frequencies. The tri-state function enables the output to go high impedance. The surface mountable J-leaded plastic package is ideal for automated assembly.

Applications & Features

- Ideally suited for high speed graphics, CISC and RISC processors, and custom ASICs
- Compact surface mountable package
- Matches EIA standard SO-J-20 footprint
- High frequencies up to 110 MHz including 106.25 MHz for Fiber Channel
- ACMOS, HCMOS and TTL compatible
- Tri-state output
- Output is short-circuit protected

Output Waveform



Frequency Range:	32 MHz to 110 MHz
Frequency Stability:	±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, aging, shock and vibration.

Temperature Range:	
Operating:	0 to +70°C or -40 to +85°C
Storage:	-55 to +125°C

Supply Voltage:	
Operating:	+5V ±10%

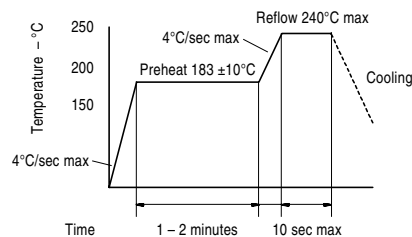
Supply Current:	50mA typ, 70mA max
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Output Specifications:	
<u>ACMOS/TTL</u>	
Symmetry:	See Part Numbering Guide
Rise & Fall Times:	2ns max, 20% to 80% VDD (ACMOS) 1ns max, 0.5 to 2.5V (TTL)
Logic 0:	10% VDD max
Logic 1:	90% VDD min
Load:	50Ω ACMOS or 10TTL
Jitter:	8ps max RMS period jitter, 1ps max 1σ cycle-to-cycle jitter

Mechanical:	
Shock:	MIL-STD-883, Method 2002, Condition B
Solderability:	MIL-STD-883, Method 2003
Terminal Strength:	MIL-STD-202, Method 211, Conditions A & C
Vibration:	MIL-STD-883, Method 2007, Condition A
Solvent Resistance:	MIL-STD-202, Method 215
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition I or J

Environmental:	
Thermal Shock:	MIL-STD-883, Method 1011, Condition A
Moisture Resistance:	MIL-STD-883, Method 1004

Solder Reflow Guide



Technical Data

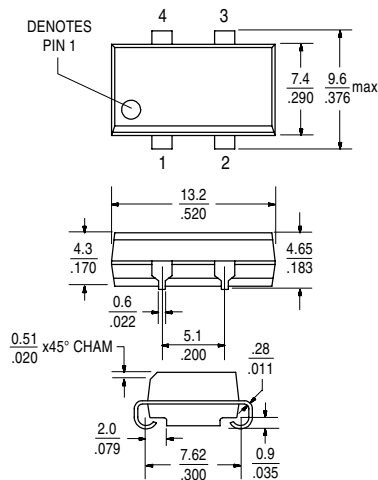
STA / STT Series, Type F

Tri-State Logic Table

Pin 1 Input	Pin 3 Output
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance

Required Input Levels on Pin 1:
 Logic 1 = 2.5V min
 Logic 0 = 0.5V max

Package Details



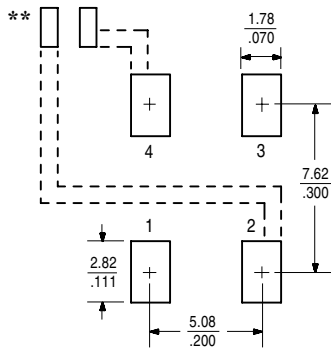
Pin Function:

Pin 1: Tri-State Control Pin 3: Output
 Pin 2: GND Pin 4: V_{DD}

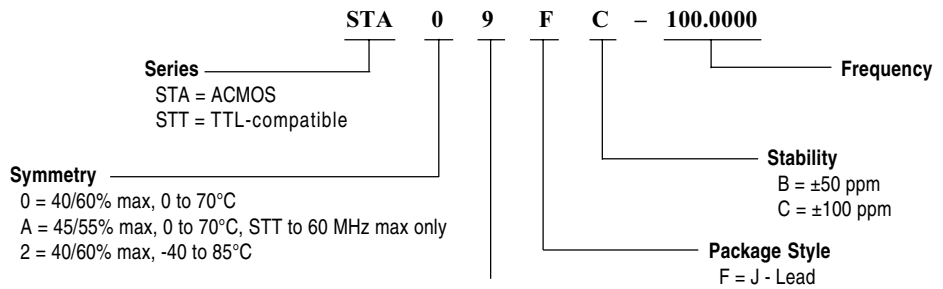
Marking Format*



Recommended Land Pattern



Part Numbering Guide

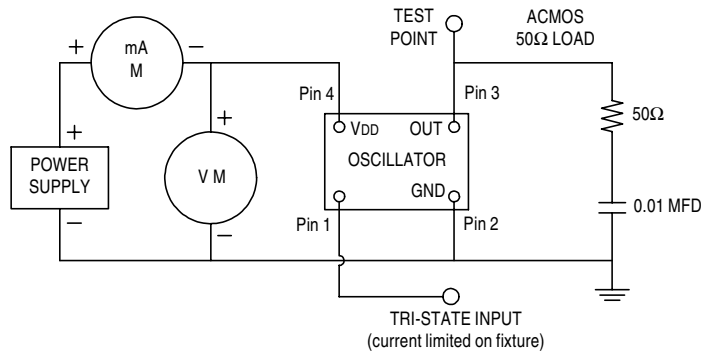


Rise/Fall Times

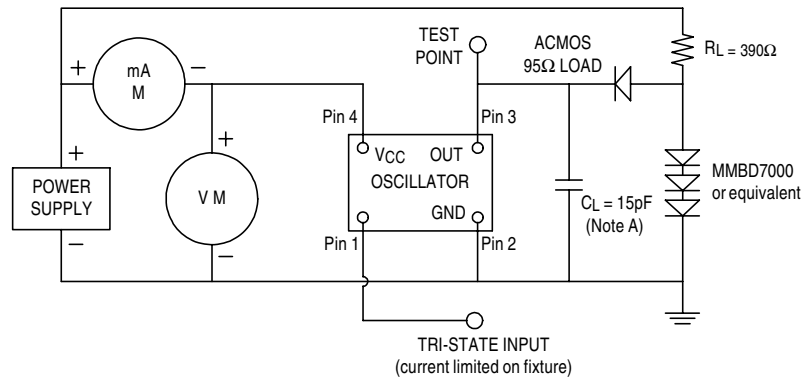
3 = 0.5ns typ, 1.0ns max for TTL
 9 = 1.0ns typ, 2.0ns max for ACMOS

Example P/N: STA09FC - 80.0000

Test Circuits



NOTE: A. CL includes probe and fixture capacitance
FIGURE 1 - ACMOS TEST FIXTURE



NOTE: A. CL includes probe and fixture capacitance
FIGURE 2 - TTL TEST FIXTURE

All specifications are subject to change without notice.